WHAT IS CLAIMED IS:

1. A voltage reference generator including a bipolar transistor configured to amplify a base current of the bipolar transistor, the base current being proportional to an absolute temperature.

2. The voltage reference generator, as recited in claim 1, wherein the base current is proportional to a voltage difference between two base-emitter voltages biased at different current densities, the voltage difference formed across a resistor coupled to the base of the bipolar transistor.

3. The voltage reference generator, as recited in claim 1, wherein a reference voltage produced by the voltage reference generator is proportional to a parabolic function of temperature.

4. The voltage reference generator, as recited in claim 1, wherein the bipolar transistor is a low-beta transistor.

5. The voltage reference generator, as recited in claim 4, wherein beta is less than ten.

6. The voltage reference generator, as recited in claim 4, wherein beta is less than five.

7. The voltage reference generator, as recited in claim 1, wherein a power supply coupled to the voltage reference generator is less than 1.7V.

8. The voltage reference generator, as recited in claim 7, wherein a power supply rejection ratio of the voltage reference generator is at least 60dB.

9. The voltage reference generator, as recited in claim 1, wherein a reference voltage generated is less than the bandgap voltage of silicon.

10. An integrated circuit comprising:

a first bipolar transistor;

a second bipolar transistor;

a resistor coupled to a base of the second bipolar transistor wherein a voltage difference between a base-emitter voltage of the first bipolar transistor and a base-emitter voltage of the second bipolar transistor forms across the resistor; and

a voltage reference node receiving a voltage based at least in part on the voltage difference.

11. The integrated circuit, as recited in claim 10, wherein a first current is based at least in part on an amplified base current of the second bipolar transistor, the base current being proportional to an absolute temperature.

12. The integrated circuit, as recited in claim 10, wherein the second bipolar transistor operates at a current density different from the current density of the first bipolar transistor.

13. The integrated circuit, as recited in claim 10, wherein the second bipolar transistor is a low-beta transistor.

14. The integrated circuit, as recited in claim 13, wherein beta is less than ten.

15. The integrated circuit, as recited in claim 13, wherein beta is less than five.

16. The integrated circuit, as recited in claim 10, further comprising:

a circuit coupled to the voltage reference node, the circuit generating a first voltage, the first voltage proportional to a complement of the absolute temperature.

17. The integrated circuit, as recited in claim 10, further comprising:

an operational amplifier maintaining effective equivalence of a voltage on a node coupled to the first bipolar transistor and a node coupled to the second bipolar transistor.

18. The integrated circuit, as recited in claim 17, wherein a noise component on the voltage reference node is substantially equivalent to noise of the operational amplifier.

19. The integrated circuit, as recited in claim 10, wherein the integrated circuit includes a maximum of one feedback path.

20. The integrated circuit, as recited in claim 11, further comprising:

a current mirror coupled to the voltage reference node, the current mirror mirroring the first current without substantially amplifying the first current.

21. The integrated circuit, as recited in claim 10, wherein the voltage is proportional to a parabolic function of temperature.

22. The integrated circuit, as recited in claim 21, wherein the resistor has a value adjusting an effective slope of the reference voltage as a function of temperature.

23. The integrated circuit, as recited in claim 10, wherein a power supply coupled to the voltage reference node is less than 1.7V.

24. The integrated circuit, as recited in claim 23, wherein the power supply rejection ratio is at least 60dB.

25. The integrated circuit, as recited in claim 10, wherein the voltage is less than the bandgap voltage of silicon.

26. A method for generating a reference voltage comprising:

developing a base current of a first bipolar transistor, the base current being proportional to absolute temperature;

amplifying the base current; and

generating a reference voltage based at least in part on the amplified base current.

27. The method, as recited in claim 26, wherein the base current is proportional to a voltage difference between a base-emitter voltage of a second bipolar transistor and a base-emitter voltage of the first bipolar transistor, the voltage difference being formed across a first resistor coupled to a base of the first bipolar transistor.

28. The method, as recited in claim 26, wherein the reference voltage is proportional to a parabolic function of temperature.

29. The method, as recited in claim 28, further comprising:
adjusting an effective slope of the reference voltage as a function of temperature according to a first resistor.

30. The method, as recited in claim 26, further comprising:
maintaining substantial equivalence of a voltage on a first node and a voltage on a second node with an operational amplifier, the first and second nodes used to develop the base current.

31. The method, as recited in claim 26, further comprising:
mirroring the amplified current, the mirroring having an effective gain of one.

32. The method, as recited in claim 27, wherein the first bipolar transistor is a low-beta transistor.

33. The method, as recited in claim 32, wherein beta is less than ten.

34. The method, as recited in claim 32, wherein beta is less than five.

35. The method, as recited in claim 26, wherein the reference voltage is less than the bandgap voltage of silicon.

36. The method, as recited in claim 26, wherein power supply coupled to the voltage reference node is less than 1.7V.

37. The method, as recited in claim 36, wherein the power supply rejection ratio is at least 60dB.

38. A computer readable medium encoding an integrated circuit product comprising:

a first bipolar transistor;

a second bipolar transistor;

a resistor coupled to a base of the second bipolar transistor wherein a voltage difference between a base-emitter voltage of the first bipolar transistor and a base-emitter voltage of the second bipolar transistor forms across the resistor; and

a voltage reference node receiving a voltage based at least in part on the voltage difference.

39. The computer readable medium encoding an integrated circuit product, as recited in claim 38, wherein a first current is based at least in part on an amplified base current of the second bipolar transistor, the base current being proportional to an absolute temperature.

40. A method of manufacturing an integrated circuit comprising:

forming a first bipolar transistor;

forming a second bipolar transistor;

forming a resistor coupled to a base of the second bipolar transistor wherein a voltage difference between a base-emitter voltage of the first bipolar transistor and a base-emitter voltage of the second bipolar transistor forms across the resistor; and

forming a voltage reference node receiving a voltage based at least in part on the voltage difference.

41. The method, as recited in claim 40, further comprising:

a first current is based at least in part on an amplified base current of the second bipolar transistor, the base current being proportional an absolute temperature.

42. The method, as recited in claim 40, wherein the second bipolar transistor operates at a current density different from the current density of the first bipolar transistor.

43. The method, as recited in claim 40, wherein the first bipolar transistor is a low-beta transistor.

44. The method, as recited in claim 40, wherein beta is less than ten.

45. The method, as recited in claim 40, wherein beta is less than five.

46. The method, as recited in claim 40, further comprising:

forming a circuit coupled to the voltage reference node, the circuit generating a first voltage, the first voltage proportional to a complement of the absolute temperature.

47. The method, as recited in claim 40, further comprising:

forming an operational amplifier maintaining effective equivalence of a voltage on a node coupled to the first bipolar transistor and a node coupled to the second bipolar transistor.

48. The method, as recited in claim 47, wherein a noise component on the voltage reference node is substantially equivalent to noise of the operational amplifier.

49. The method, as recited in claim 41, further comprising:

forming a current mirror coupled to the voltage reference node, the current mirror mirroring the first current without substantially amplifying the first current.

50. The method, as recited in claim 40, wherein the voltage is proportional to a parabolic function of temperature.

51. The method, as recited in claim 50, wherein the resistor has a value adjusting an effective slope of the reference voltage as a function of temperature.

52. The method, as recited in claim 40, wherein a power supply coupled to the voltage reference node is less than 1.7V.

53. The method, as recited in claim 52 wherein the power supply rejection ratio is at least 60dB.

54. The method, as recited in claim 40, wherein the voltage is less than the bandgap voltage of silicon.

55. An apparatus comprising:

means for developing a base current of a bipolar transistor, the base current being proportional to absolute temperature;

means for amplifying the base current; and

means for generating a reference voltage based at least in part on the amplified base current.

56. The apparatus, as recited in claim 55, wherein the voltage varies according to a parabolic function of temperature.

57. The method, as recited in claim 55, further comprising:

means for adjusting an effective slope of the reference voltage as a function of temperature.